APPENDIX I - PENDING CLAIMS

SYSTEM SUPPORTING MULTIPLE MEMORY MODES
INCLUDING A BURST EXTENDED DATA OUT MODE

Appellant: Brett L. Williams
Serial No.: 09/510,375

26. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the fast page mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

27. The system of claim 26, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

28. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of

a mode selected from the group consisting of burst extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the fast page mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

29. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and extended data out mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the extended data out mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set

of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

30. The system of claim 29, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

31. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and extended data out mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the extended data out mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the

memory includes data read from the memory device.

32. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signals and the second set of access control signals to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

33. The system of claim 32, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

34. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for

operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signals and the second set of access control signals to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

35. A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank.

36. The system of claim 35, wherein the memory type of the second bank is interchangeable.

37. A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory.

38. A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank, the access control signals being driven in the first and second modes in response to information obtained by reading the first and second banks, respectively.

39. A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank and a second bank, wherein the first bank and the second bank are

each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory, and controls access of the first bank in accordance with one of the first and second sets of requirements based on information obtained by reading the first bank, and controls access of the second bank in accordance with one of the first and second sets of requirements based on information obtained by reading the second bank.

40. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

41. The system of claim 40, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power

up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

42. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller, wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

43. A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second modes.

44. The system of claim 43, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second modes.

45. A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory includes a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements.

46. The system of claim 45, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second sets of requirements.

47. A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank, the access control signals being driven in the first and second modes in response to information obtained by reading the first and second banks, respectively;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second modes.

48. The system of claim 47, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second modes.

49. A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory includes a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory, and controls access of the first bank in accordance with one of the first and second sets of requirements based on information obtained by reading the first bank, and controls access of the second bank in accordance with one of the first and second sets of requirements based on information obtained by reading the second bank;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements and to program the memory controller in accordance with the first and second sets of requirements.